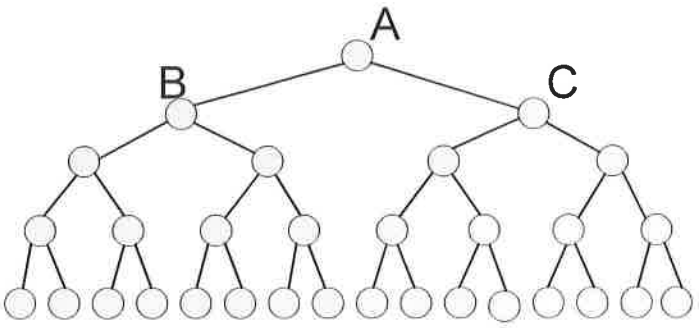
Problem 1.

On a complete binary tree of 2^k-1 nodes, assign integers 1, 2, 3, ..., 2^k-2, 2^k-1 to the 2^k-1 nodes such that no two nodes will be assigned with a same integer. Calculate how many ways of assignment are there such that a node is always assigned with an integer larger than that assigned to its child nodes. An example of a complete binary tree with k = 5 is shown below, where node B and node C are child nodes of node A.

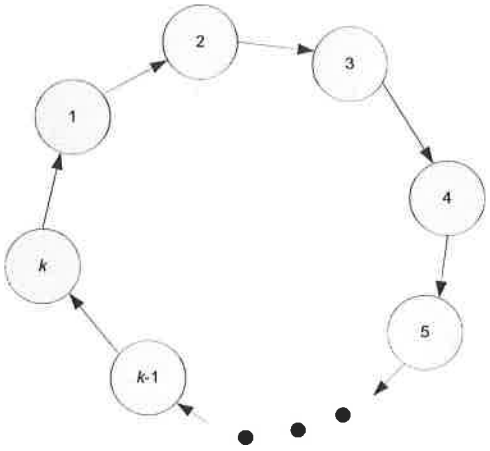


Problem 2.

For the following graph (a ring of *k* nodes, where *k* is a positive integer), let a *k*-by-*k* matrix *M* be defined as follows:

$m_{i,j} = 1$ if there exists an edge from node *i* to node *j*; otherwise, $m_{i,j} = 0$, where $m_{i,j}$ is the element of *M* at *i*th row and *j*th column. For example, if *k* = 4, $M = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix}$.

Prove that $M^a = M^{a \bmod k}$, where *a* is a positive integer. As an example, $M^3 = M \times M \times M$. If you think M^a possesses some special physical meaning, you need to prove that first.



Problem 3.

Given the following program:

```
void main()
{
  int i,j,k,n,z;
  double x=0,y=0;
  cin >> n;  //get value from user
  for (i=1;i<=n;i++)
  {
    z=i-((i/2)*2);
    if (z==1)
    {
      for (j=i; j<=n; j++)
        x=x+1;
      for (k=1; k<=i; k++)
        y=y+1;
    }
  }
}
```

What is the overall complexity of the above code in terms of n? You need to show your calculation.

Problem 4.

Consider a class Two34_tree for 2_3_4 trees, with member functions add and remove.

Show intermediate diagrams for the following add and remove operations.

```
two34_tree t1;
t1.add(40);
t1.add(30);
t1.add(20);
t1.add(100);
t1.add(120);
t1.add(200);
t1.add(400);
t1.add(600);
t1.add(800);
t1.remove(20);
t1.remove(200);
t1.remove(100);
```

Problem 5.

Consider a processor with 8KB data cache which is 2-way set-associative. Each cache line holds 32B data. The memory address has 32 bits with bit 0 representing the MSB and bit 31 representing the LSB.

(1) How many tag bits are needed for this data cache? Assume tag field is located at the MSB of the address.

(2) Consider the following piece of C code:

```
for (i = 0; i < 4; i++)
    {
      x = data3[i];
      for (j = 0; j < 4; j++)
        {
         /* multiply data1 rows by data2 columns */
         x += data1[ i ][ j ] * data2[ j ][ i ];
        }
      data3[i] = x;
    }
```

Above, data1 and data 2 are both 4x4 integer arrays; data3 is a 1x4 vector. The starting addresses of data1, data2 and data3 are 0x14F40, 0x14FA0 and 0x15000, respectively. Assume this is the first time these data are accessed. Variables *i*, *j*, and *x* are mapped to registers during compilation (i.e. there is no memory access when read and write those variables.) What is the cache hit rate for executing this piece of code?

Consider a pipelined processor with 5 stages: IF (Instruction Fetch), ID (Instruction decode/register file read), EX (Execute/address calculation), MEM (Memory access) and WB (register file write back). The register file has 2 read ports and 1 write port. Assume that the instruction set consists only 4 types of instructions: ADD (add the contends of two registers and store the result in the third one), BEQ (branch if the contend of two registers are equal), LW (load the memory contend to a register) and SW (store the contend of a register to a memory location). Moreover the profiled probabilities of their occurrences are: ADD (50%), BEQ (20%), LW (25%), SW (5%).

(1) Assume there are no stalls, and all instructions in a program are independent random variables. How often (percentage of cycles) do we need to use all three register ports in the same cycle?

(2) Consider the following assembly codes.

```
ADD   R5, R2, R1    //$R5=$R2+$R1
LW    R4, 4(R5)     //$R4=MEMORY[4+$R5]
LW    R2, 0(R2)     //$R2=MEMORY[$R2]
ADD   R3, R5, R3    //$R3=$R5+$R3
SW    R3, 0(R5)     //MEMORY[$R5]=$R3
```

The initial value in R1, R2, R3, R4 and R5 are 0x10, 0x20, 0x30 0x40 and 0x50 respectively. The memory is initialized so that each byte in the memory stores an unsigned value that equals the lower 8 bit (8 bit LSB) of its address. For example, the byte at address 0x01234576 has the value 0x76. The processor is big Endian. What will be the content in register R1~R5 after running the assembly instructions? If there is a memory write, which memory entry is modified, to what value?

(3) The assembly codes in (2) are written under the assumption that the processor has forwarding and hazard detection capability. Assume that the processor has no forwarding and hazard detection (but still with the aforementioned 5-stage pipeline architecture), will the register and memory content be updated according to the programmer's original intention (i.e. with the assumption that hazard detection and forwarding capability is available)? Explain why or why not? If your answer is no, please modify the program by inserting NOPs and/or re-arranging instructions so that it generates the expected result. If your answer is yes, can the execution time be reduced by re-arranging the instructions?

Problem 7.

Consider a computer A. Its CPI for ALU instructions, control instructions and memory instructions are 1, 1.5, and 2 respectively. We also know that in a program, there are 50% ALU instructions, 10% control instructions and 40% memory instructions.

(1) If the clock frequency of computer A is 5MHz, and there are 100,000 instructions in the program. What is the CPU time to execute this program?

(2) If there is another computer B, its clock frequency is 10MHz and its MIPS rate is 2 when running the same program. Which computer is faster, A or B?

Problem 8.

DO ALL WORK ON THESE PAGES

Controller Design (Finite-State Machine Design)

Implement the following use-case description using combinational logic and a state register.

Use case description: Create a completely specified deterministic three-state FSM with a single input x and a single output y with the following behavior:

1. The initial state is S_0. If the machine is in S_0, then the output y is 0. If the input x is 0, the machine changes to state S_1. If the input x is 1, the machine changes to state S_2.
2. If the machine is in state S_1, the output y is 0. If x is 0, the next state is S_0. If x is 1, the next state is S_2.
3. If the machine is in state S_2, the output y is 1. If the input x is 0, the next state is S_2. If x is 1, the next state is S_0.

Fully document each stage of your design by including:

1. A state-transition diagram,
2. A truth table whose inputs are the current machine state and input variables, and whose outputs are the next-state functions and output functions, and
3. Logical formulas for next-state and output functions specifying the combinational logic necessary to implement the machine.

Use the standard binary coding for your state encoding, i.e.,

$$S_0 = s_1s_0 = 00,\ S_1 = s_1s_0 = 01,\ S_2 = s_1s_0 = 10$$

Important: for the unused state encoding $s_1s_0 = 11$, regardless of input value the next state should be S_0 and the output y should be 0.

(a) State-Transition Diagram

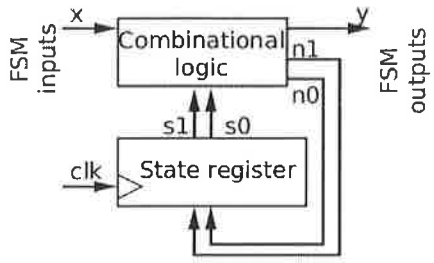
DO ALL WORK ON THESE PAGES

(b) Next-state and output truth table

Present State, Input			Next State, Output		
s1	s0	x	n1	n0	y
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

(c) Implementation using a state register and combinational logic

For the architecture shown above, based the next-state and output truth table, write the logical formulas that define $n_1(s_1, s_0, x)$, $n_0(s_1, s_0, x)$, and $y(s_1, s_0)$. Note: **minimization is not necessary**.



$n_1(s_1, s_0, x) =$

$n_0(s_1, s_0, x) =$

$y(s_1, s_0) =$

Problem 9.

DO ALL WORK ON THESE PAGES

Datapath Performance, Timing, and Control

Consider the (non-pipelined) datapath consisting of two registers and two combinational multipliers with its associated FSM controller. Notice that the FSM controller sets output *rdy* to **1** one clock cycle before the first valid outputs emerge, and *rdy* remains **1** until the next reset.

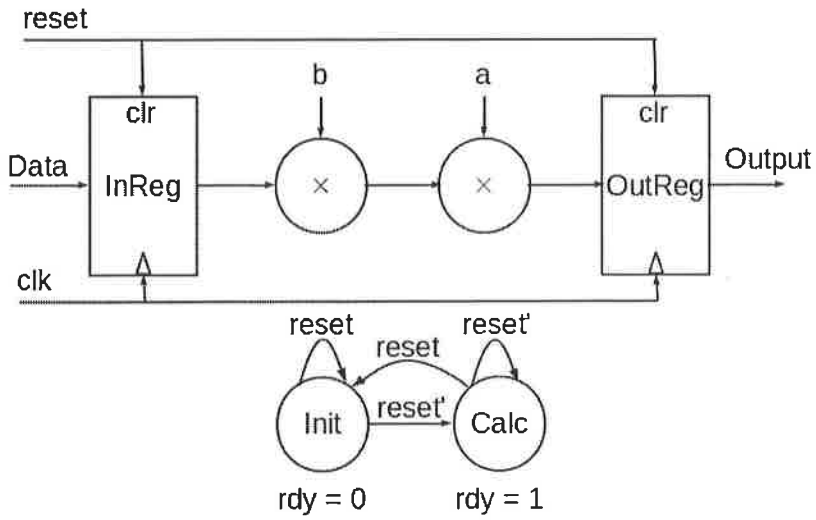


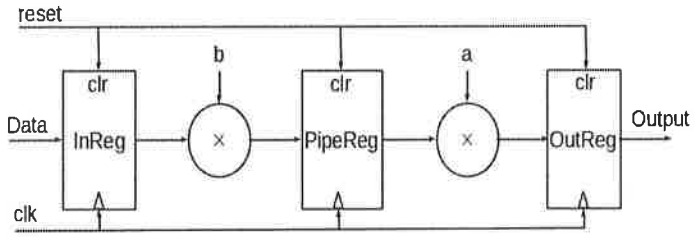
Figure 1: Non-Pipelined Datapath with FSM Controller

(a) Based on the datapath and finite-state state machine control in Figure 1, fill in the timing diagram below

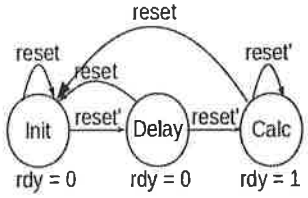
Clock Period	0	1	2	3	4	5	6	7	8
reset	1	1	0	0	0	1	0	0	0
Current State	x								
Next State									
Data	x	x	v0	v1	v2	v3	v4	v5	v6
InReg									
Output									
rdy									

DO ALL WORK ON THESE PAGES

(b) Timing Diagram for Pipelined Design



(a) Pipelined Datapath



(b) FSM Controller for Pipelined Datapath

Figure 2: Pipelined Datapath with FSM Controller

Consider the pipelined datapath above in Figure 2(a), which inserts a register (PipeReg) in the datapath and its associated FSM Controller in Figure 2(b). Fill in the table below

Clock Period	0	1	2	3	4	5	6	7	8
reset	1	0	0	0	1	0	0	0	0
Current State	x								
Next State									
Data	x	v0	v1	v2	v3	v4	v5	v6	v7
InReg									
PipeReg									
Output									
rdy									

(c) Performance Comparison

Suppose that the each multiplication takes 100 nanoseconds. Fill in the performance table below.

Design	Minimum clock period (ns)	Throughput (ns) minimum time between inputs	Latency (ns) Time from input stored into InReg to output appearing in OutReg
non-pipelined			
pipelined			

(d) Which design is faster, i.e., produces more results in the same amount of time? Circle the correct answer.

(A) Pipelined (B) Non-Pipelined (C) Both are equally fast

Problem 10

A small spherical cavity of radius a is carved out of a dielectric material with permittivity ε which is placed between two very large conducting plates. The voltage V_o is applied between the two conducting plates. Assuming the thickness of the dielectric slab is $d >> a$, find the electric field inside the cavity as well as in the dielectirc.

(a) First find the electric field in the dielectric, in the absence of the cavity. Assume the field is uniform.

(b) Now adding a cavity, find the electric fields inside the air cavity and in the dielectric, by solving for the potential distributions in each region.

Problem 11

A hollow cylinder (tube) of inner and outer radii a, b and infinite length carries the non-uniform volume current density **J:**

$$\mathbf{J} = \mathbf{a}_z J_o\left(\frac{\rho}{a}\right) \qquad (a<\rho<b)$$

This current carrying cylinder is surrounded by a very long, coaxial cylinder (tube) of inner and outer radii b, c, filled with the magnetic material of permeability 100 μ_o.

(a) Find the magnetic field **B** (direction and magnitude) everywhere: (i) $\rho < a$, (ii) $a < \rho < b$, (iii) $b < \rho < c$, (iv) $\rho > c$.

(b) Find the volume bound current density $\mathbf{J}_m$ and the surface bound current densities $\mathbf{J}_{ms}$ at the inner ($\rho = b$) and outer ($\rho = c$) surfaces of the magnetic material.

Problems 12

A uniform plane wave in free space travels in z-direction. Its electrical field is given as $\mathbf{E}(z, t) = \mathbf{E}_x \cos(\omega t - \beta z)$, where $\mathbf{E}_x$ a constant vector in x-direction with a value of 1 V/m. The wave frequency is 400 MHz. A square metal loop of 10 cm by 10 cm with a total resistance 100 Ohm is placed on z-axis. The center of the loop is at z=2 m. Find the power on the loop for the following cases:

(a) The loop is on x-z plane

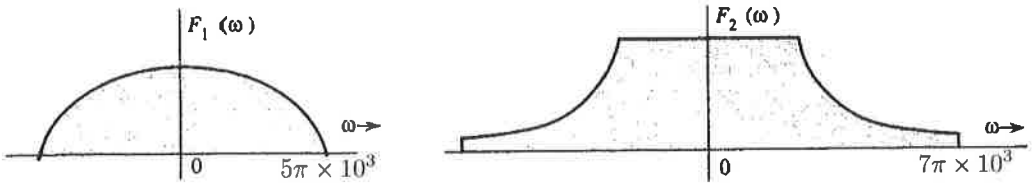
(b) The loop is on y-z plane

(c) The loop is on a plane that is formed by rotating the x-z plane by 45^0 around the z-axis

(d) The loop is on x-z plane but its center is moved to z =2.75 m

Problem 13:

The figure below shows the Fourier spectra of the signals $f_1(t)$ and $f_2(t)$.



Determine the Nyquist sampling rate for each of the following signals, fully justifying your answer in every case.

(a) $2f_1(t) + 3f_2(t)$

(b) $f_1(t)\, f_2^3(t)$

Problem 14:

Consider two signals $s_1(t)$ and $s_2(t)$, each with bandwidth W. Quadrature-carrier multiplexing is performed to send these signals simultaneously. The multiplexed signal is

$$u(t) = A_c\, s_1(t)\cos(2\pi f_c t) + A_c\, s_2(t)\sin(2\pi f_c t)$$

where A_c is the carrier amplitude and f_c is the carrier frequency. Assume that $f_c > 2W$.

a) Express the Fourier transform $U(f)$ of $u(t)$ in terms of the Fourier transforms of $s_1(t)$ and $s_2(t)$. (You can use the modulation property of the Fourier transform given below.)

b) In order to recover $s_1(t)$ at the receiver, $u(t)$ first gets multiplied with $\cos(2\pi f_c t)$ and then goes through an ideal lowpass filter with frequency response

$$H_{\text{LPF}}(f) = \begin{cases} 1 & |f| \le W \\ 0 & \text{otherwise} \end{cases}.$$

Determine the output of the lowpass filter.

c) Discuss how the other signal $s_2(t)$ can be recovered at the receiver.

Useful Facts

1. $\cos(2\pi f_0 t) = \frac{1}{2}(e^{j2\pi f_0 t} + e^{-j2\pi f_0 t})$
2. $\sin(2\pi f_0 t) = \frac{1}{2j}(e^{j2\pi f_0 t} - e^{-j2\pi f_0 t})$
3. Modulation property of the Fourier Transform:

   $$\mathcal{F}[x(t)e^{j2\pi f_0 t}] = X(f - f_0)$$

   where $X(f) = \mathcal{F}[x(t)]$ denotes the Fourier Transform of $x(t)$.
4. $\cos a \cos b = \frac{1}{2}[\cos(a+b) + \cos(a-b)]$.
   $\sin a \sin b = \frac{1}{2}[\cos(a-b) - \cos(a+b)]$
   $\sin a \cos b = \frac{1}{2}[\sin(a+b) + \sin(a-b)]$

Problem 15:

A continuous time signal is given below:

$$x(t) = \cos 500\pi t + \cos 1600\pi t \tag{1}$$

You are asked to design a DSP system that consists of the following components:

- A sampling device with a sampling frequency f_s;
- An ideal lowpass filter with a cutoff frequency f_c;

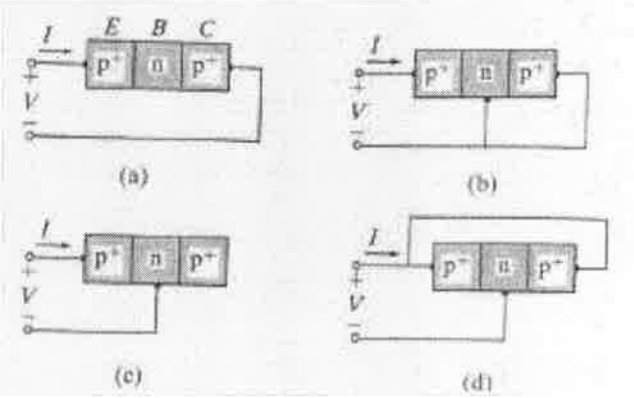
Your goal is to generate a new signal $y(t) = A\cos 400\pi t$, where A can be any positive number, by applying the system to the given signal $x(t)$ in (1).

1. Determine a pair of design parameters, f_s and f_c, that achieve the design objective.
2. Find a *different* pair of (f_s, f_c) to achieve the same design objective.

In both cases, you need to justify why it works using the frequency spectrum plot.

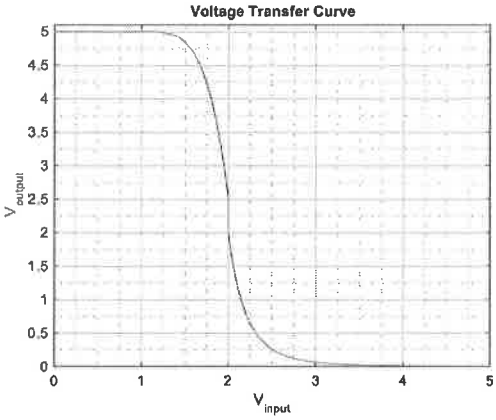
Problem 16

The symmetrical p+-n-p+ transistor is connected as a diode in the four configurations as shown below. Assume that V >> kT/q. Sketch $\delta p(x_n)$ (excess hole concentration as a function of distance in the base) in the base region for each case. Which connection seems most appropriate for use as a diode and why?

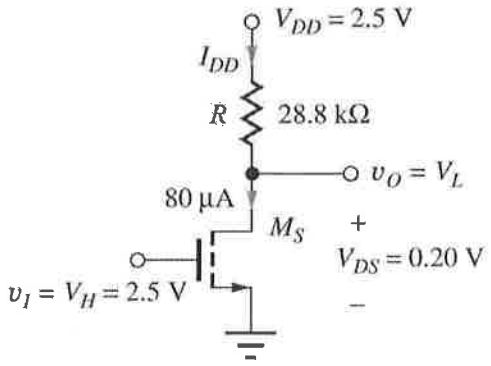


Problem 17

a) Using the transfer curve below, estimate the noise margin of the logic gate (note, this is graphical, not computational, approximations are acceptable).



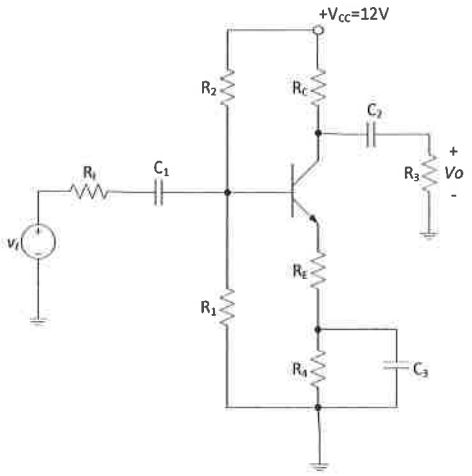
b) For V_L=0.2V at the output of the NMOS inverter with V_{TN}=0.6V and K_n'=100x10^{-6}, I_{DD}=80 μA, V_{DD}=V_H=2.5 V, what is W/L? Explain your answer.



c) If the output of the inverter in part b) is connected to a 10 pF capacitor, what is the associated fall time?

Problem 18

Common Emitter Amplifier:



Parameter	*Value*
β_f	100
g_m	9.8 mS
r_π	10.2 kΩ
r_o	320 kΩ
R_1	160 kΩ
R_2	300 kΩ
R_3	50 kΩ
R_4	10 kΩ
R_E	5 kΩ
R_C	22 kΩ
R_I	25 kΩ
C_1	1 pF
C_2	1 pF
C_3	1 pF

(a) Draw the small signal model of this circuit.

(b) What is the voltage gain of this circuit?